CLAIMS:

What is claimed is:

1. A method of processing a multi-precision shift instruction, comprising:

fetching and decoding a multi-precision shift instruction;

executing the multi-precision shift instruction on an operand within a multi-word value to shift the operand and concatenate the shifted value with bits shifted out of a previous shift operation on the same multi-word value; and

outputting the result.

2. The method according to claim 1, further comprising storing the bits shifted out of the operand during the executing into a carry register.

3. The method according to claim 1, wherein the multi-precision shift instruction is a shift left instruction.

4. The method according to claim 1, wherein the multi-precision shift instruction is a shift right instruction.

5. The method according to claim 1, wherein the concatenation step is performed by a logical OR operation.

6. The method according to claim 1, wherein the multi-precision shift instruction specifies a shift increment.

7. The method according to claim 6, wherein the shift increment is greater than or equal to the number of bits in a word.

8. The method according to claim 6, wherein the shift increment is less than the number of bits in a word.

9. A processor for processing multi-precision shift instructions, comprising:

a program memory for storing instructions including a multi-precision shift instruction;

a program counter for identifying current instructions for processing; and

a barrel shifter for executing shift instructions, the barrel shifter including:

a carry register for storing values shifted out of sections of the barrel shifter; and

OR logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter,

the barrel shifter executing a shift instruction fetched from the program memory to a) load an operand into a section within the barrel shifter, b) shift the operand, c) output the shifted value and d) store into the carry register bits shifted out of the section of the barrel shifter.

10. The processor according to claim 9, wherein the barrel shifter executes a multi-precision shift instruction to further e) concatenate the value in the carry register with the shifted operand prior to outputting the shifted value.

11. The processor according to claim 9, wherein the shift instruction is a shift left instruction.

12. The processor according to claim 9, wherein the shift instruction is a shift right instruction.

13. The processor according to claim 9, wherein the shift instruction is an arithmetic shift instruction.

14. The processor according to claim 9, wherein the shift instruction is a logical shift instruction.

15. The processor according to claim 9, wherein the shift instruction specifies a shift increment.

16. The processor according to claim 9, wherein the barrel shifter executes at least two shift instructions to shift a multi-word value.

17. The processor according 16, wherein the first instruction of the at least two shift instructions is not a multi-precision shift instruction.

18. The processor according 16, wherein the second and subsequent instructions of the at least two shift instructions is a multi-precision shift instruction.